SPECIFICATIONS

All specifications at T_A = +25°C, $\pm V_{CC}$ = $\pm V_{DD}$ = ±5V, f_S = 768kHz (96kHz × 8), and 24-bit data, unless otherwise noted.

		PCM1704U			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION			24		Bits
DATA FORMAT					
Audio Data Interface Format			20-, 24-Bit, MSB-First		
Audio Data Code			Binary Two's Complement		
Sampling Frequency (f_S)		16		96	kHz
Input Clock Frequency				25	MHz
DIGITAL INPUT/OUTPUT					
Input Logic Level:					
V_{IH}(1)		+2.0		±5.0	V
V_{IL}(1)		0		+0.8	V
V_{IH}(2)		–3.0		0	V
V_{IL}(2)		–5.0		–4.2	V
Input Logic Current:					
I_{IH}(1)	V_{IH} = $+V_{DD}$			±10	μA
I_{IL}(1)	V_{IL} = 0V			±10	μA
I_{IH}(2)	V_{IH} = 0V			±10	μA
I_{IL}(2)	V_{IL} = $-V_{DD}$			–100	μA
DYNAMIC PERFORMANCE(3)					
THD+N at V_O = 0dB	PCM1704U		0.0025	0.0030	%
	PCM1704U-J		0.0015	0.0025	%
	PCM1704U-K		0.0008	0.0015	%
THD+N at V_O = –20dB	PCM1704U		0.008	0.020	%
	PCM1704U-J		0.007	0.015	%
	PCM1704U-K		0.006	0.01	%
Dynamic Range	EIAJ, A-weighted				
	PCM1704U, -U-J	102	110		dB
	PCM1704U-K	106	112		dB
Signal-to-Noise Ratio	EIAJ, A-weighted	112	120		dB
Low Level Linearity	f = 1002Hz at –90dB		±0.5		dB
DC ACCURACY					
Gain Error			±1.0	±3.0	% of FSR

PCM1704

Integrated circuits
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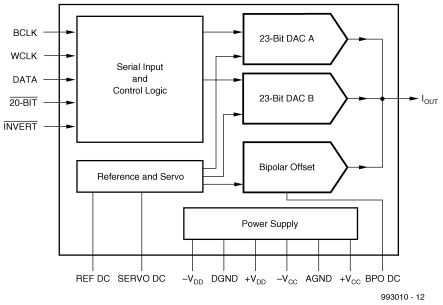
PCM1704
Soundplus™ 24-Bit, 96 kHz BiCMOS Sign-Magnitude Digital-to-Analog Converter

Manufacturer
Burr-Brown,
P.O. Box 1140,
Tucson, AZ 85734, U.S.A.
Tel. (520) 746-1111, fax (520) 889-1510.
Internet: http://www.burr-brown.com/

Features
- Sampling frequency (f_s): 16 kHz to 96 kHz
- 8x oversampling at 96 kHz
- Input audio data word: 20-, 24-bit
- High performance:
  - dynamic range: K grade = 112dB typ
  - SNR: 120dB typ
  - THD+N: K grade = 0.0008% typ
- Fast current output: ±1.2mA/200ns
- Glitch-free output
- Pin-programmable data inversion
- Power supply: ±5V
- Small 20-lead so package

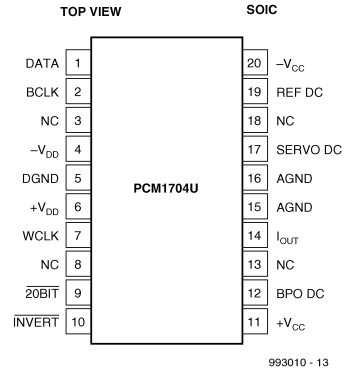
Application Example
Audio DAC2000,
Elektor Electronics November 1999 – January 2000

Description
The PCM1704 is a precision, 24-bit digital-to-analog converter with exceptionally high dynamic performance. The ultra-low distortion and excellent low-level signal performance makes the PCM1704 an ideal candidate for high-end consumer and professional audio applications. When used with a digital interpolation filter, the PCM1704 supports 8× oversampling at 96kHz.
The PCM1704 incorporates a BiCMOS sign-magnitude architecture that eliminates glitches and other nonlinearities around bipolar zero. The PCM1704 is precision laser-trimmed at the factory to minimize differential linearity and gain errors.



PCM1704 Block Diagram.

In addition to high-performance audio systems, the PCM1704 is well suited to waveform synthesis applications requiring very low distortion and noise.



Pin configuration, top view, SOIC

Audio Data Interface

Basic Operation
The audio interface of the PCM1704 accepts TTL-compatible input levels. The data format at the DATA input of the PCM1704 is Binary Two's Complement, with the most significant bit (MSB) being first in the serial input bit stream. Table I shows the relationship between the audio input data and DAC output for the PCM1704. Any number of bits can precede the 24

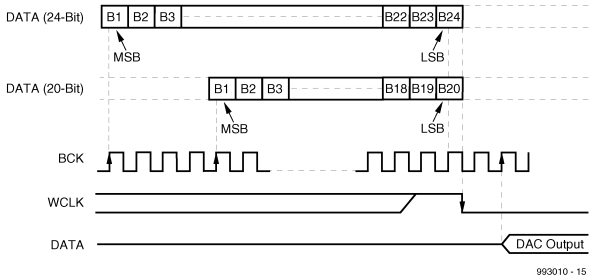


Figure 1. Audio input data format

bits to be loaded since only the last 24 bits will be transferred to the parallel DAC register after WCLK (pin 7) has gone LOW (logic 0).

BINARY TWO'S COMPLEMENT INPUT DATA (Hex)	DAC OUTPUT
7FFFFF	+ Full Scale
000000	Bipolar Zero
FFFFFF	Bipolar Zero – 1 LSB
800000	– Full Scale

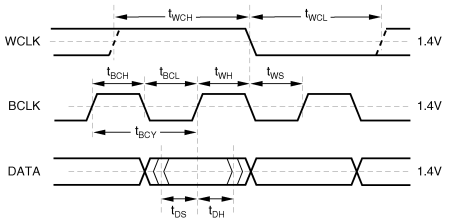
Table I. Digital Input/DAC Output Relationships.

Audio data is supplied to the DATA (pin 1) input. The bit clock is used to shift data into the PCM1704 and is supplied to BCLK (pin 2). All DAC serial input data bits are latched into the serial input register on the rising edge of BCLK. The serial-to-parallel data transfer to the DAC occurs on the falling edge of WCLK.

The change in the output of the DAC occurs at the rising edge of the 2nd BCLK after the falling edge of WCLK. Figure 1 shows the audio data input format. Figure 2 shows the input timing relationships.

Maximum Bit Clock (BCLK) Rate
The maximum BCLK rate is specified as 25MHz. This is derived from the 8× oversampling of the PCM1704. Given a 96kHz sampling rate, an 8× oversampling input and a 32-bit frame length, we get: 96kHz × 8 × 32 = 24.576MHz

'Stopped Clock' Operation
The PCM1704 is normally operated with a continuous BCLK input. If BCLK is stopped between input data words, the last 24 bits shifted in are not actually transferred from the serial register to the parallel DAC register until WCLK goes LOW. WCLK must remain LOW until after the first BCLK cycle of the next data word to insure proper DAC operation. The specified setup and hold times for DATA and WCLK must be observed.



BCLK Pulse Cycle Time	t_{BCY}	40ns	(min)
BCLK Pulse Width HIGH	t_{BCH}	14ns	(min)
BCLK Pulse Width LOW	t_{BCL}	14ns	(min)
BCLK Rising Edge to WCLK Falling Edge	t_{WH}	10ns	(min)
WCLK Falling Edge to BCLK Rising Edge	t_{WS}	10ns	(min)
WCLK Pulse Width HIGH	t_{WCH}	> t_{BCY}	
WCLK Pulse WIdth LOW	t_{WCL}	> t_{BCY}	
DATA Set-up Time	t_{DS}	10ns	(min)
DATA Hold Time	t_{DH}	10ns	(min)

Figure 2. Audio input data timing

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		PCM1704U			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Bipolar Zero Error			±0.5	±1.0	% of FSR
Gain Drift	0ºC to 70ºC		±25		ppm of FSR/ºC
Bipolar Zero Error Drift	0ºC to 70ºC		±5		ppm of FSR/ºC
ANALOG OUTPUT					
Output Range			±1.2		mA
Output Impedance			1.0		kΩ
Settling Time	±0.0003% of FSR, ±1.2mA Step		200		ns
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC} = +V_{DD}$		+4.75	+5.0	+5.25	VDC
Voltage Range: $-V_{CC} = -V_{DD}$		–4.75	–5.0	–5.25	VDC
Combined Supply Current: $+I_{CC}$	$+V_{CC} = +V_{DD} = +5.0V$		5	8	mA
Combined Supply Current: $-I_{CC}$	$-V_{CC} = -V_{DD} = -5.0V$		30	45	mA
TEMPERATURE RANGE					
Operation		–25		+85	ºC
Storage		–55		+125	ºC

NOTES:
(1) BCLK, WCLK, DATA.
(2) $\overline{20BIT}$, $\overline{INVERT}$.
(3) Dynamic performance data is tested with 5534 I/V amp with 7.5kΩ feedback resistor. THD+N data is tested by Shibasoku 725C with 30kHz external LPF, 400Hz HPF, average mode. Input signal frequency = 1.1kHz.

Data format control
Data format is controlled by two pins on the PCM1704—the $\overline{20BIT}$ and $\overline{INVERT}$ inputs. Their functions are described in the following paragraphs and tables.

Input Word Length
$\overline{20BIT}$ (pin 9) is used to select the input data length. Table II shows the available selections. Pin 9 is internally pulled up to DGND and therefore, defaults to 24-bit data.

Input Data Inversion
$\overline{INVERT}$ (pin 10) is used to select the phase of the input data presented to the DAC. Table III shows the two options. Pin 10 is internally pulled up to DGND, and therefore defaults to normal, or non-inverting data.

$\overline{20BIT}$ (Pin 9)	DATA WORD LENGTH
$\overline{20BIT}$ = H (DGND)	24-Bit Data Word
$\overline{20BIT}$ = L (–VDD)	20-Bit Data Word

Table II. Input Word Length Selection.

$\overline{INVERT}$ (Pin 10)	PHASE
$\overline{INVERT}$ = H (DGND)	Normal (non-inverted)
$\overline{INVERT}$ = L ($-V_{DD}$)	Inverted

Table III. Input Data Phase Selection.